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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/674,771	09/30/2003	Mark Visokay	TI-35943	4450

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EXAMINER	
KENNEDY, JENNIFER M	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 07/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/674,771	VISOKAY ET AL.	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) *1-28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *29-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/2003, 12/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election of claims 29-41 in the reply filed on May 7, 2004 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claims 1-28 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 35-41 are rejected under 35 U.S.C. 102(b) as being anticipated by Bertrand et al. (U.S. Patent No. 6,432,817).

In re claim 35, Bertrand discloses a transistor gate structure, comprising a gate dielectric (21) formed above a semiconductor body;

a first metal silicide (23) above the gate dielectric, the first metal silicide being doped with n or p-type impurities (see column 4, lines 49-50); and

a second metal silicide (40) above the first metal silicide.

In re claim 36, Bertrand et al. discloses the device wherein the first and second metal silicides are different (23, 40, see column 5, lines 20-35).

In re claim 37, Bertrand discloses the device further comprising silicon between the first and second metal silicides. The examiner notes, that as interpreted as broadly as possible, silicon atoms would be present in the interface between the tungsten silicide layer and the nitride silicide layer of Bertrand et al. Further, the examiner notes that one could consider the first half of the tungsten silicide layer to be the first metal silicide layer and the second half of the tungsten silicide layer of Bertrand et al. to be the silicon as claimed, since the tungsten silicide layer contains silicon. Similarly, the examiner could consider the first half of the nickel silicide layer to be the silicon, and the second half of the nickel silicide layer to be the second metal silicide layer.

In re claims 38 and 39, Bertrand et al. discloses the device wherein the first metal silicide comprises a refractory metal, and wherein the refractory metal is one of molybdenum, tungsten, tantalum, and titanium (23, tungsten silicide).

In re claims 40 and 41, Bertrand et al. discloses the device wherein the second metal silicide comprises nickel (40, nickel silicide).

Claims 29-33, 35, 38-41 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsumoto (U.S. Patent No. 6,432,817).

In re claim 29, Matsumoto discloses a semiconductor device comprising:

an NMOS transistor gate structure, the NMOS gate structure comprising a gate dielectric (12) above a semiconductor body, an n-doped first metal silicide structure above the gate dielectric, and a second metal silicide above the n-doped first metal silicide (18, see column 5, lines 40-65); and

a PMOS transistor gate structure, the PMOS gate structure comprising a gate dielectric (12) above a semiconductor body, a p-doped first metal silicide structure above the gate dielectric, and a second metal silicide above the p-doped first metal silicide (see column 5, lines 40-65).

The examiner notes that the metal silicide layer 18 can be considered a first and a second metal silicide layer. The examiner is considering the first half to be the first metal silicide layer and the second half to be the second silicide layer. The examiner notes that since the two layers are not required to be different in material a single layer can be considered two layers of the same layer.

In re claims 30 and 31, Matsumoto discloses the device wherein the first metal silicide comprises a refractory metal, and wherein the refractory metal is one of molybdenum, tungsten, tantalum, and titanium (see column 5, lines 56-65).

In re claim 32, Matsumoto discloses the device wherein the second metal silicide comprises nickel (see column 5, lines 56-65).

In re claim 33, Matsumoto discloses the device further comprising silicon between the first and second metal silicides in the NMOS and PMOS gate structures.

The examiner notes, that as interpreted as broadly as possible, the first one third of the silicide layer 18 could be considered the first metal silicide layer, the second third to be the silicon as claimed and the last third to be the second metal silicide layer.

In re claim 35, Matsumoto discloses a transistor gate structure, comprising

a gate dielectric (12) formed above a semiconductor body;

a first metal silicide (first half of 18) above the gate dielectric, the first metal silicide being doped with n or p-type impurities; and

a second metal silicide (second half of 18) above the first metal silicide.

The examiner notes that the metal silicide layer 18 can be considered a first and a second metal silicide layer. The examiner is considering the first half to be the first metal silicide layer and the second half to be the second silicide layer. The examiner notes that since the two layers are not required to be different in material a single layer can be considered two layers of the same layer.

In re claims 38 and 39, Matsumoto discloses the device wherein the first metal silicide comprises a refractory metal, and wherein the refractory metal is one of molybdenum, tungsten, tantalum, and titanium (see column 5, lines 56-65).

In re claims 40 and 41, Matsumoto discloses the device wherein the second metal silicide comprises nickel (see column 5, lines 56-65).

Claims 29-33, 35, 38-41 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakajima et al. (U.S. Patent No. 5,444,302).

In re claim 29, Nakajima et al. discloses a semiconductor device comprising:

an NMOS transistor gate structure, the NMOS gate structure comprising a gate dielectric (5) above a semiconductor body, an n-doped first metal silicide structure above the gate dielectric, and a second metal silicide above the n-doped first metal silicide (see column 3, lines 20-40, column 11, lines 3-9, column 13, lines 4-11, column 17, line 50 through column 19, line 51, and Figures 2-14); and

a PMOS transistor gate structure, the PMOS gate structure comprising a gate dielectric (5) above a semiconductor body, a p-doped first metal silicide structure above the gate dielectric, and a second metal silicide above the p-doped first metal silicide (see column 3, lines 20-40, column 11, lines 3-9, column 13, lines 4-11, column 17, line 50 through column 19, line 51, and Figures 2-14).

In re claims 30 and 31, Nakajima et al. discloses the device wherein the first metal silicide comprises a refractory metal, and wherein the refractory metal is one of molybdenum, tungsten, tantalum, and titanium (see column 19, lines 60-69).

In re claim 32, Nakajima et al. discloses the device wherein the second metal silicide comprises nickel (see column 19, lines 60-69).

In re claim 33, Nakajima et al. discloses the device further comprising silicon between the first and second metal silicides in the NMOS and PMOS gate structures. The examiner notes, that as interpreted as broadly as possible, one of the metal silicide layers formed can be considered the silicon since silicide comprises silicon.

In re claim 35, Nakjima et al. discloses a transistor gate structure, comprising

a gate dielectric (5) formed above a semiconductor body;

a first metal silicide above the gate dielectric, the first metal silicide being doped with n or p-type impurities; and

a second metal silicide above the first metal silicide (see column 3, lines 20-40, column 11, lines 3-9, column 13, lines 4-11, column 17, line 50 through column 19, line 51, and Figures 2-14) .

In re claim 38 and 39, Nakjima et al. discloses the device wherein the first metal silicide comprises a refractory metal, and wherein the refractory metal is one of molybdenum, tungsten, tantalum, and titanium (see column 19, lines 60-69).

In re claims 40 and 41, Nakjima et al. discloses the device wherein the second metal silicide comprises nickel (see column 19, lines 60-69).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 29-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto (U.S. Patent No. 5,877,535) in view of Bertrand et al. (U.S. Patent No. 6,432,817).

In re claim 29, Matsumoto discloses a semiconductor device comprising:

an NMOS transistor gate structure, the NMOS gate structure comprising a gate dielectric (12) above a semiconductor body, an n-doped first metal silicide structure above the gate dielectric (18, see column 5, lines 40-65); and

a PMOS transistor gate structure, the PMOS gate structure comprising a gate dielectric (12) above a semiconductor body, a p-doped first metal silicide structure above the gate dielectric (see column 5, lines 40-65).

Masumoto does not discloses the method of forming a second metal silicide over the first metal silicide in both the NMOS and PMOS regions.

Bertrand et al. discloses forming a second metal silicide (40) over a first metal silicide (23, see column 5, lines 20-35). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a gate electrode with two silicide layers, a first metal silicide and a second metal silicide in the NMOS and PMOS regions because as Bertrand et al. discloses, the gate electrode with two silicide layers enable the formation of a nickel silicide on polycrystalline silicon while preventing a complete silicidation of the polycrystalline silicon gate electrode so as to preserve the work function of the polysilicon and the polysilicon/silicon dioxide interface. The examiner notes that Bertrand et al. discloses that the technique is useful for various types of devices and particularly useful in highly integrated devices with MOS transistors.

In re claims 30 and 31, Bertrand et al. discloses the device wherein the first metal silicide comprises a refractory metal, and wherein the refractory metal is one of molybdenum, tungsten, tantalum, and titanium (23, tungsten silicide).

In re claim 32, Bertrand et al. discloses the device wherein the second metal silicide comprises nickel (40, nickel silicide).

In re claim 33, Bertrand et al. discloses the device further comprising silicon between the first and second metal silicides in the NMOS and PMOS gate structures.

The examiner notes, that as interpreted as broadly as possible, silicon atoms would be present in the interface between the tungsten silicide layer and the nitride silicide layer of Bertrand et al. Further, the examiner notes that one could consider the first half of the tungsten silicide layer to be the first metal silicide layer and the second half of the tungsten silicide layer of Bertrand et al. to be the silicon as claimed, since the tungsten silicide layer contains silicon. Similarly, the examiner could consider the first half of the nickel silicide layer to be the silicon, and the second half of the nickel silicide layer to be the second metal silicide layer.

In re claim 34, Bertrand et al. discloses the device wherein the first and second metal silicides are different 23, 40, see column 5, lines 20-35).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Bryant et al. (U.S. Patent No. 5,742,095) discloses that nickel is considered a refractory metal.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Kennedy
Patent Examiner
Art Unit 2812